# BUK9Y14-40B

## N-channel TrenchMOS logic level FET

**Rev. 03 — 2 June 2008** **Product data sheet**

# 1. Product profile

## 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP High Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

## 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating

## 1.3 Applications

- Air bag
- Automotive transmission control
- Fuel pump and injection
- Automotive ABS systems
- Diesel injection systems
- Motors, lamps and solenoids

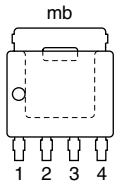
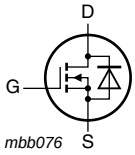
## 1.4 Quick reference data

**Table 1. Quick reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | - | - | 40 | V |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C; see Figure 4 and 1 | - | - | 56 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | - | - | 85 | W |
| **Dynamic characteristics** | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 5 V; $I_D$ = 10 A; $V_{DS}$ = 32 V; see Figure 14 | - | 9 | - | nC |
| **Static characteristics** | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 20 A; $T_j$ = 25 °C; see Figure 12 and 13 | - | 12 | 14 | mΩ |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 56 A; $V_{sup} \leq 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped | - | - | 89 | mJ |

## 2. Pinning information

**Table 2. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1, 2, 3 | S | source |   SOT669 (LFPAK) |   |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK9Y14-40B | LFPAK | plastic single-ended surface-mounted package (LFPAK); 4 leads | SOT669 |

## 4. Limiting values

**Table 4. Limiting values**

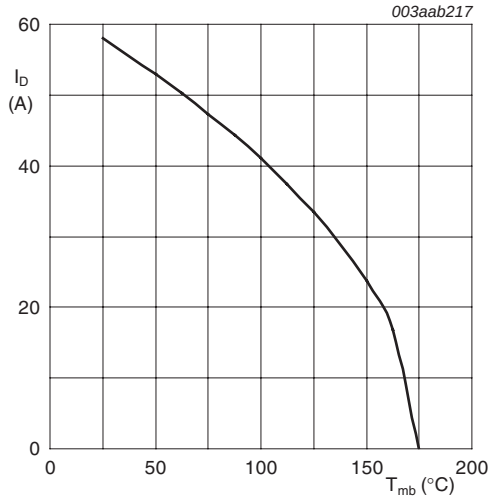
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | 40 | V |
| $V_{GS}$ | gate-source voltage | | | 15 | 15 | V |
| $I_D$ | drain current | $T_{mb} = 25$ °C; $V_{GS} = 5$ V; see Figure 4 and 1 | | - | 56 | A |
| | | $T_{mb} = 100$ °C; $V_{GS} = 5$ V; see Figure 1 | | - | 40 | A |
| $I_{DM}$ | peak drain current | $T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 4 | | - | 226 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | | - | 85 | W |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 56$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped | | - | 89 | mJ |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | see Figure 3 | [1][2] [3] | - | - | J |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb} = 25$ °C | | - | 56 | A |
| $I_{SM}$ | peak source current | $t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C | | - | 226 | A |

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

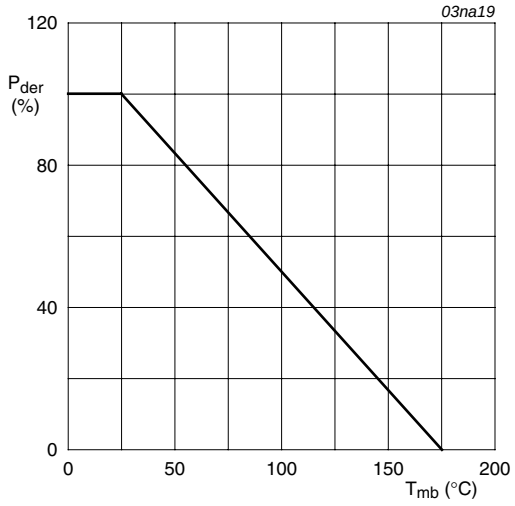
[2] Repetitive avalanche rating limited by average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.



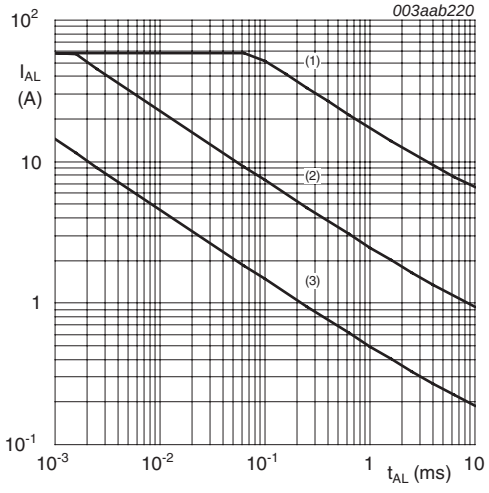

$V_{GS} \geq 5V$

**Fig 1. Continuous drain current as a function of mounting base temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

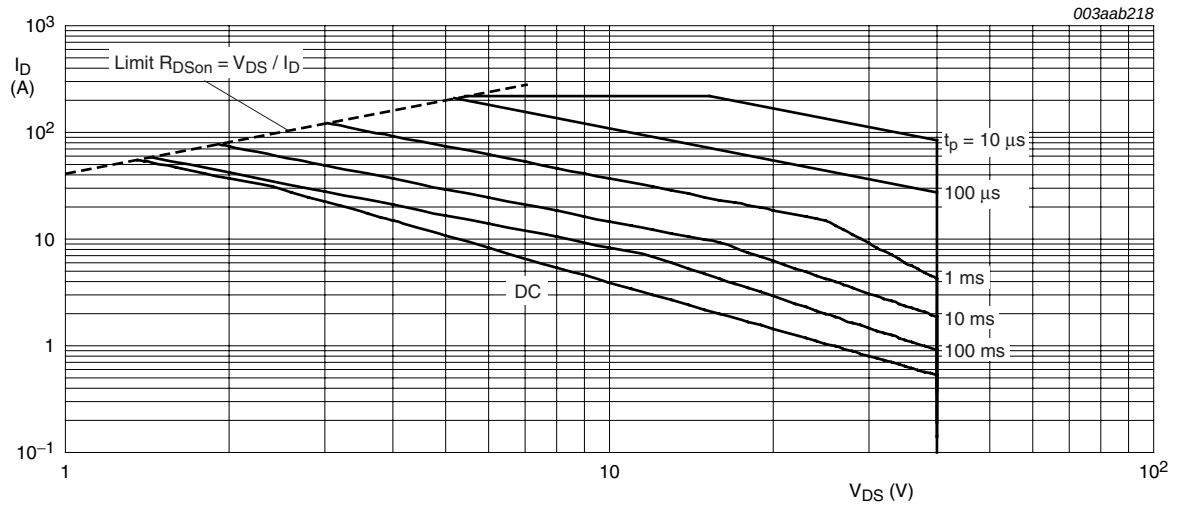



(1) Single−pulse; $T_j$ = 25 °C.

(2) Single−pulse; $T_j$ = 150 °C.

(3) Repetitive.

**Fig 3. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period**




$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse

**Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 5 | - | - | 1.8 | K/W |

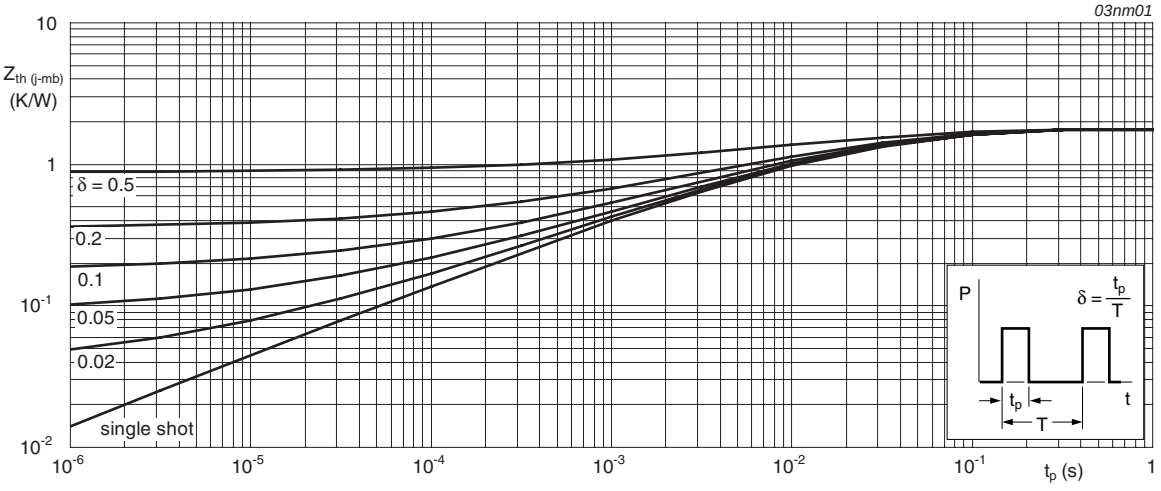
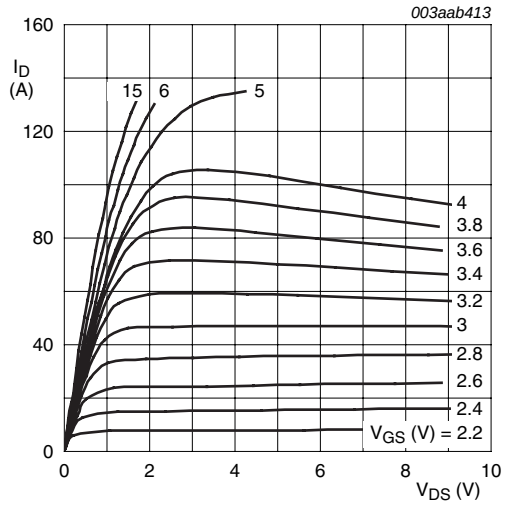



**Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

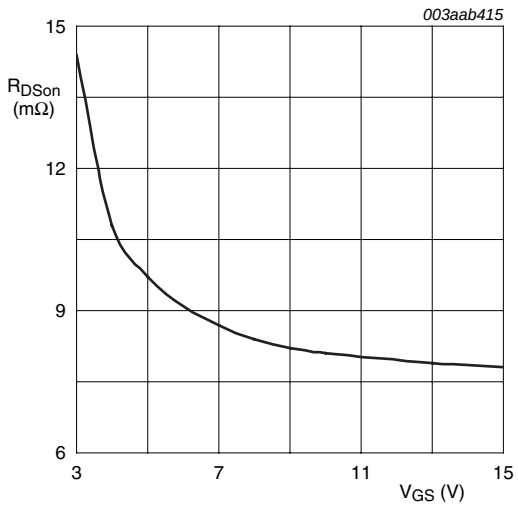
**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 μA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 40 | - | - | V |
| | | $I_D$ = 250 μA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 10 | - | - | 2.3 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 11 and 10 | 1.1 | 1.5 | 2 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; see Figure 10 | 0.5 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | - | - | 500 | μA |
| | | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.02 | 1 | μA |
| $I_{GSS}$ | gate leakage current | $V_{DS}$ = 0 V; $V_{GS}$ = 20 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| | | $V_{DS}$ = 0 V; $V_{GS}$ = -20 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 20 A; $T_j$ = 175 °C; see Figure 12 | - | - | 26 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 20 A; $T_j$ = 25 °C | - | - | 16 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 20 A; $T_j$ = 25 °C | - | 9 | 11 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 20 A; $T_j$ = 25 °C; see Figure 12 and 13 | - | 12 | 14 | mΩ |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 16 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/μs; $V_{GS}$ = 0 V; $V_{DS}$ = 30 V | - | 50 | - | ns |
| $Q_r$ | recovered charge | | - | 26 | - | nC |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 10 A; $V_{DS}$ = 32 V; $V_{GS}$ = 5 V; see Figure 14 | - | 21 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 3.7 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 9 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 15 | - | 1360 | 1800 | pF |
| $C_{oss}$ | output capacitance | | - | 274 | 330 | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 147 | 200 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 30 V; $R_L$ = 2.5 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 10 Ω | - | 15 | - | ns |
| $t_r$ | rise time | | - | 34 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 68 | - | ns |
| $t_f$ | fall time | | - | 42 | - | ns |



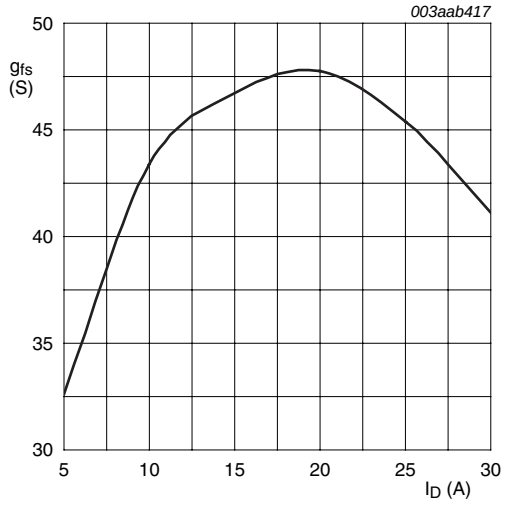

$T_j = 25\ °C$

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



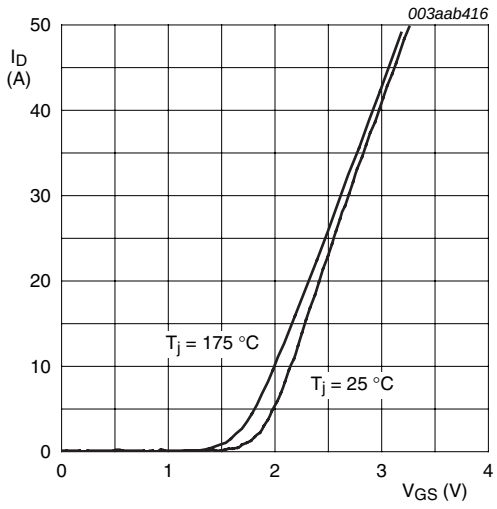

$T_j = 25\ °C; I_D = 20\ A$

**Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



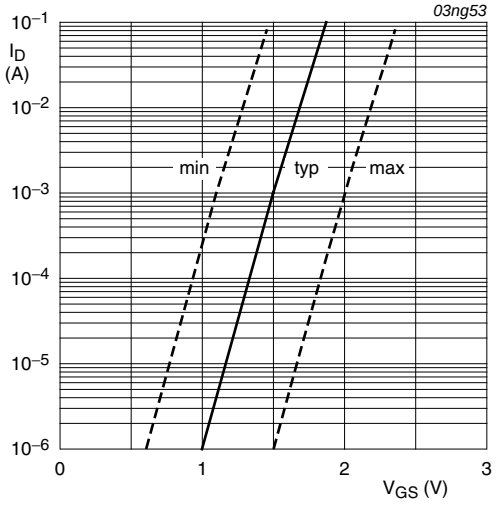

$T_j = 25\ °C; V_{DS} = 25\ V$

**Fig 8. Forward transconductance as a function of drain current; typical values**



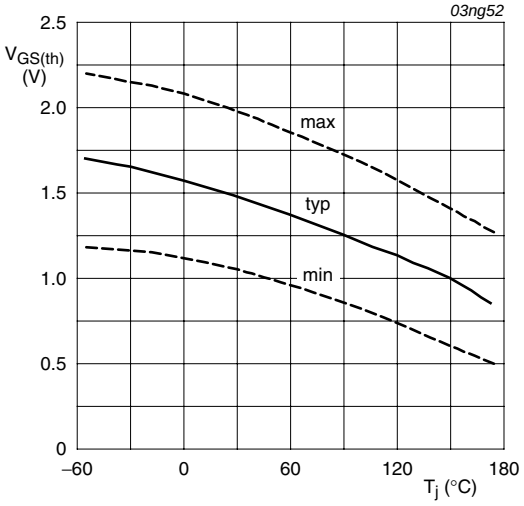

$V_{DS} = 25\ V$

**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



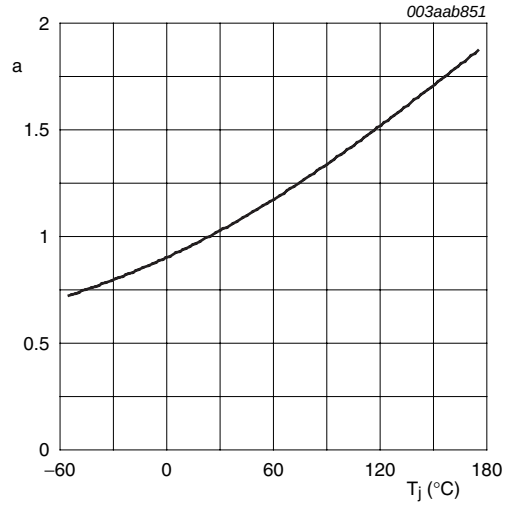

$T_j = 25\ °C; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



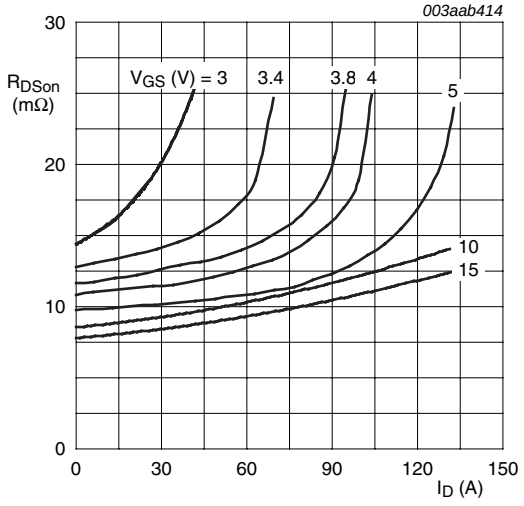

$I_D = 1\ mA; V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



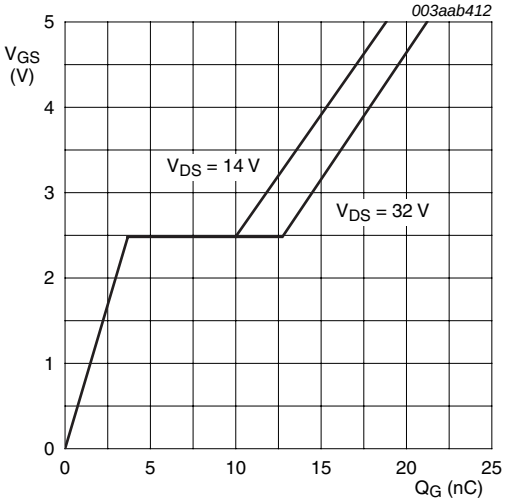

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**



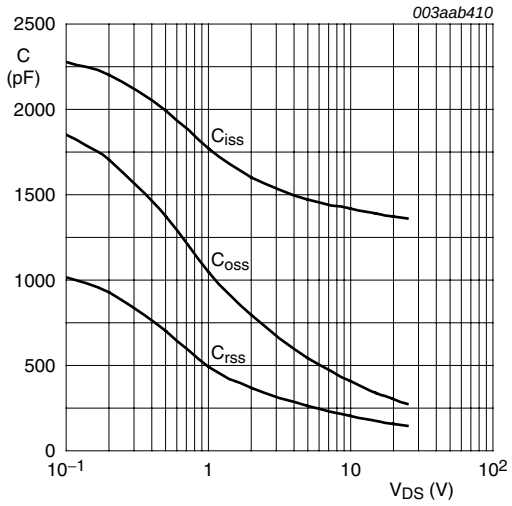

$T_j = 25\ °C$

**Fig 13. Drain-source on-state resistance as a function of drain current; typical values**



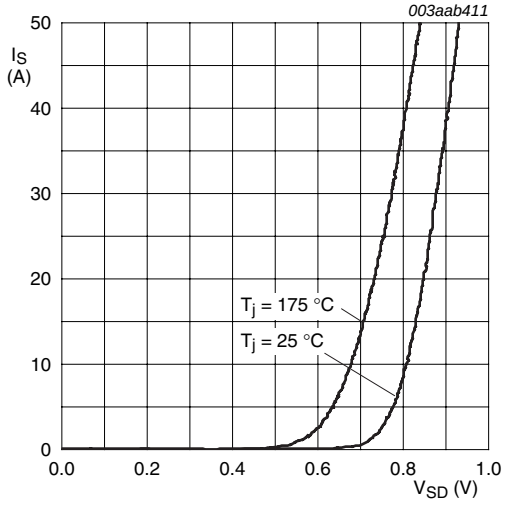

$T_j = 25\,°C; I_D = 10\,A$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**




$V_{GS} = 0\,V; f = 1\,MHz$

**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

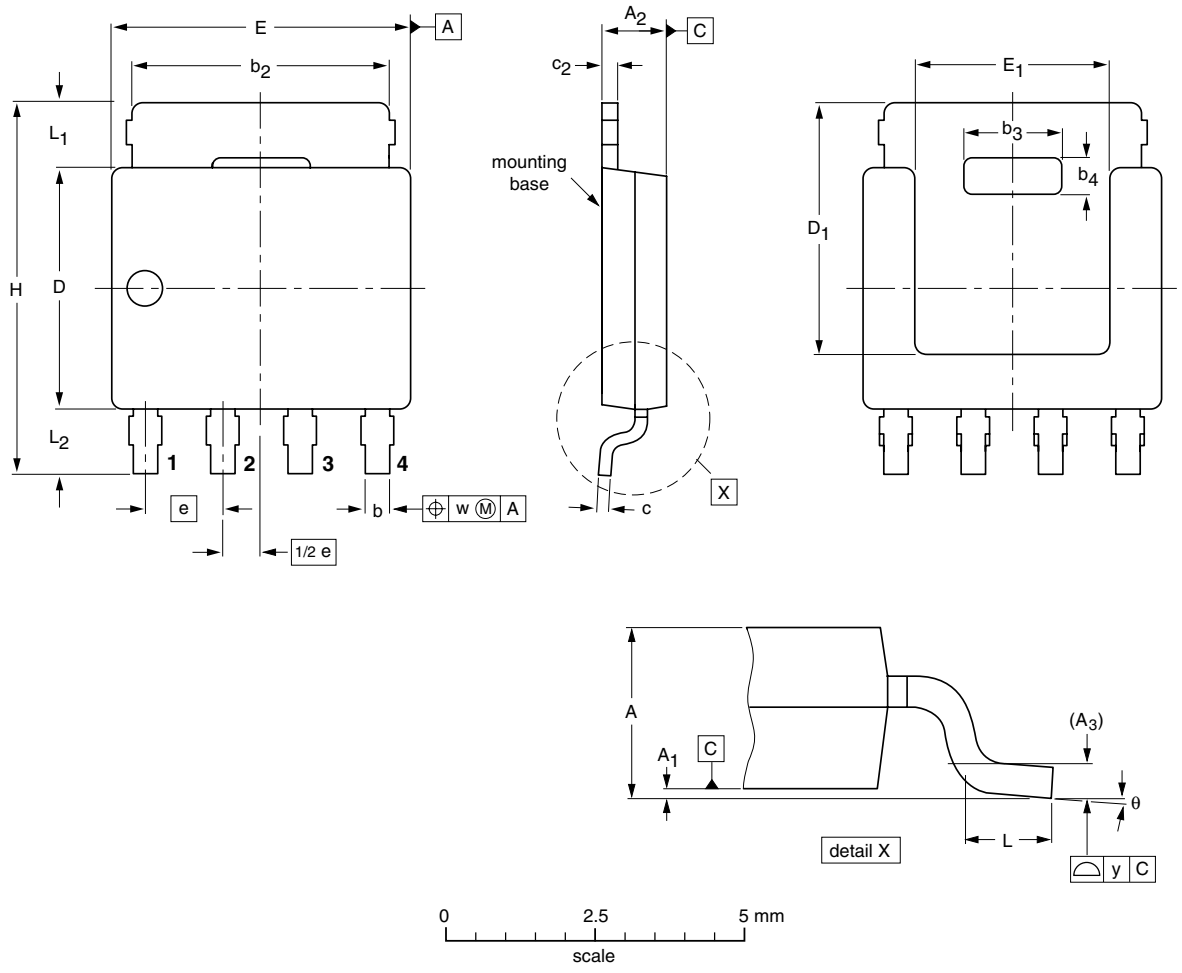



$V_{GS} = 0\,V$

**Fig 16. Source current as a function of source-drain voltage; typical values**

## 7. Package outline

**Plastic single-ended surface-mounted package (LFPAK); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 2.2<br>2.0 | 0.9<br>0.7 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~04-10-13~~<br>06-03-16 |

**Fig 17. Package outline SOT669 (LFPAK)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BUK9Y14-40B_3 | 20080602 | Product data sheet | | BUK9Y14-40B_2 |
| Modifications: | • Table 4 $V_{DS}$ temperature operating range corrected | | | |
| BUK9Y14-40B_2 | 20080523 | Product data sheet | - | BUK9Y14-40B_1 |
| BUK9Y14-40B_1 | 20070903 | Product data sheet | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 9.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 9.3 Disclaimers

**General —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Quick reference data —** The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

## 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**TrenchMOS** — is a trademark of NXP B.V.

# 10. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

## 11. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 2 June 2008**

**Document identifier: BUK9Y14-40B_3**